Lab 5 report

4:1 Multiplexer

CE 436-01

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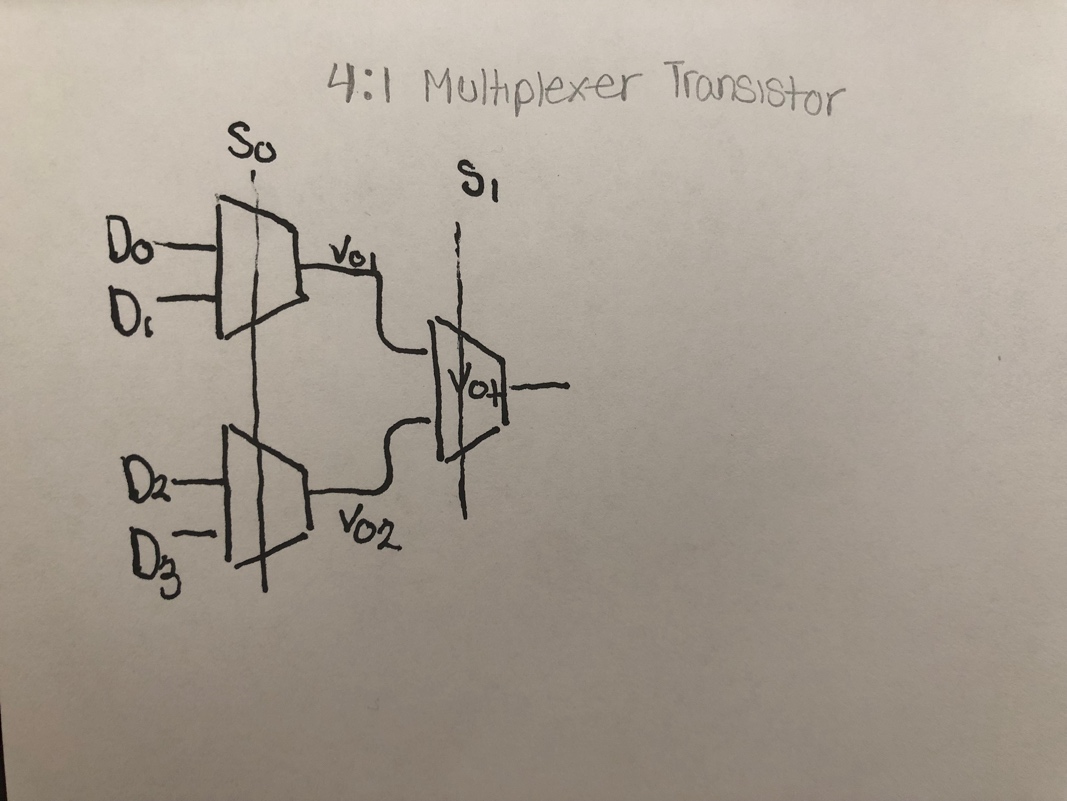
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11/15/21

**Objective:**

The objective is to create a 4:1 multiplexer, use design hierarchy to develop each circuit with Magic layout tools, and simulate each circuit with IRSIM.

The first figure shows how we were able to sketch out the transistor level of a 4:1 Multiplexer and following sketch with the second diagram is a sketch of the Stick diagram of what a 4:1 Multiplexer would look like.

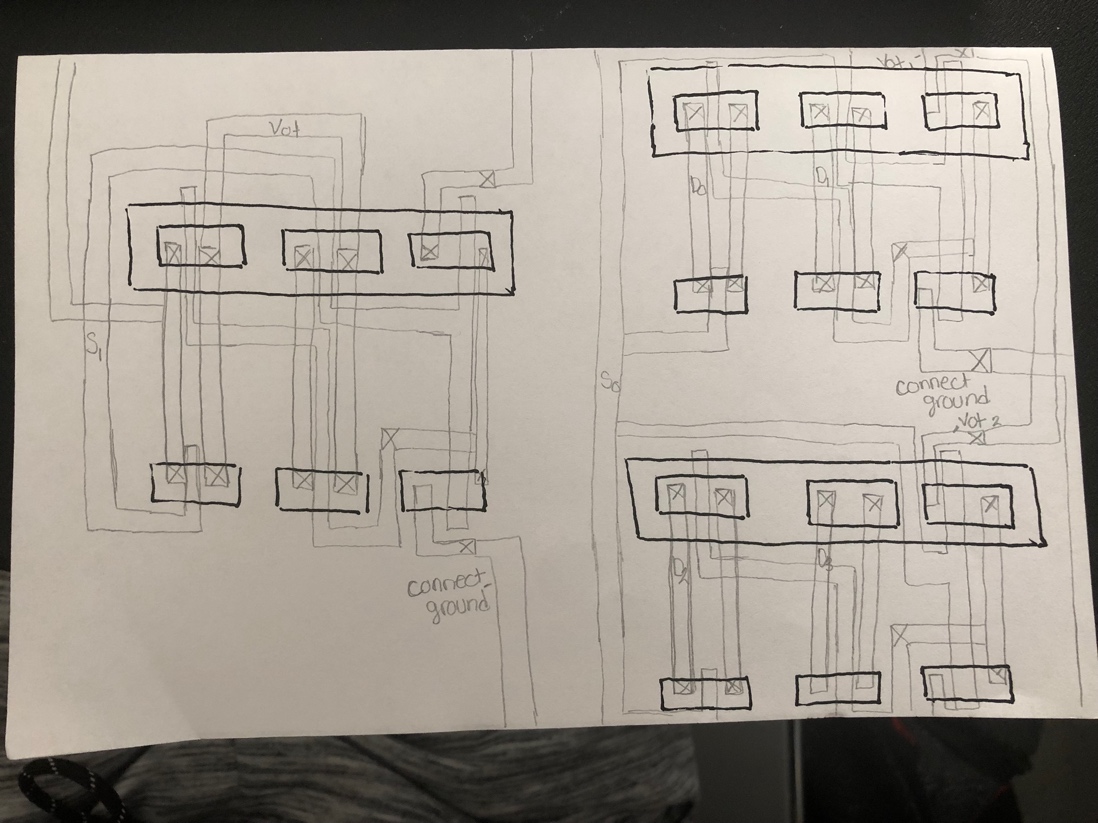
Figure 1: Transistor level diagram for a 4:1 Multiplexer

Figure 2: Stick Diagram of a 4:1 Multiplexer

There are 6 transistors in a 2:1 MUX (2x2 (transmission gates) + 2 (inverter). As a result, the 4:1 MUX contains 3x6 = 18 transistors. Therefore, we need 13 n-CMOS and 13 P-CMOS transistors to construct this 4:1 Multiplexer. As I start to implement a 4:1 Multiplexer, I will be able to go back from the sketches that I drew and so if I am on track as I go more in depth to create a 4:1 Multiplexer.

**Physical 4:1 Multiplexer**

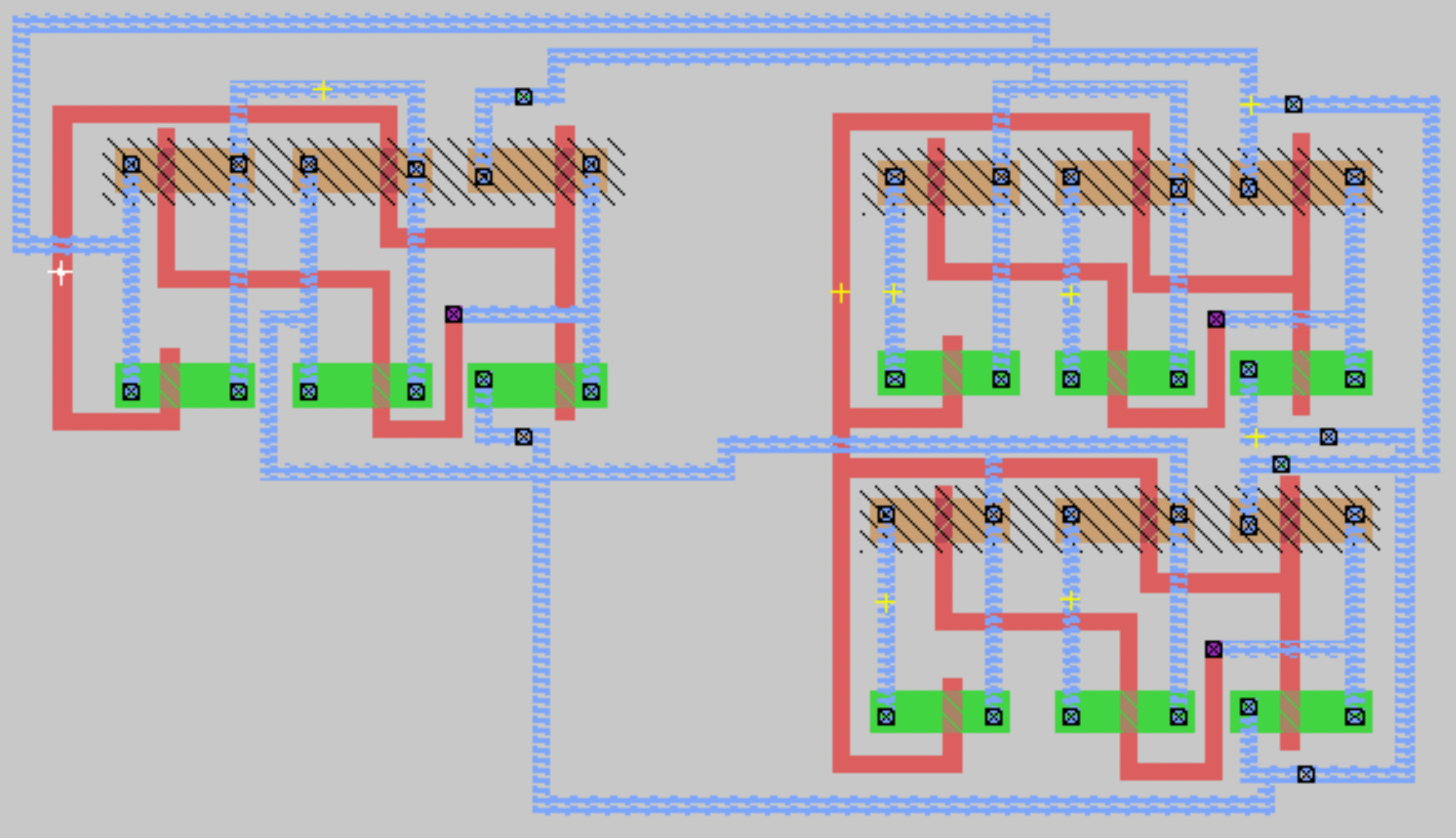
After sketching out the two figures I followed the next step which was to build a physical 4:1 Multiplexer on Magic as shown in Figure 3.

Figure 3: CMOS physical layout of a 4:1 Multiplexer

**Waveform and Output:**

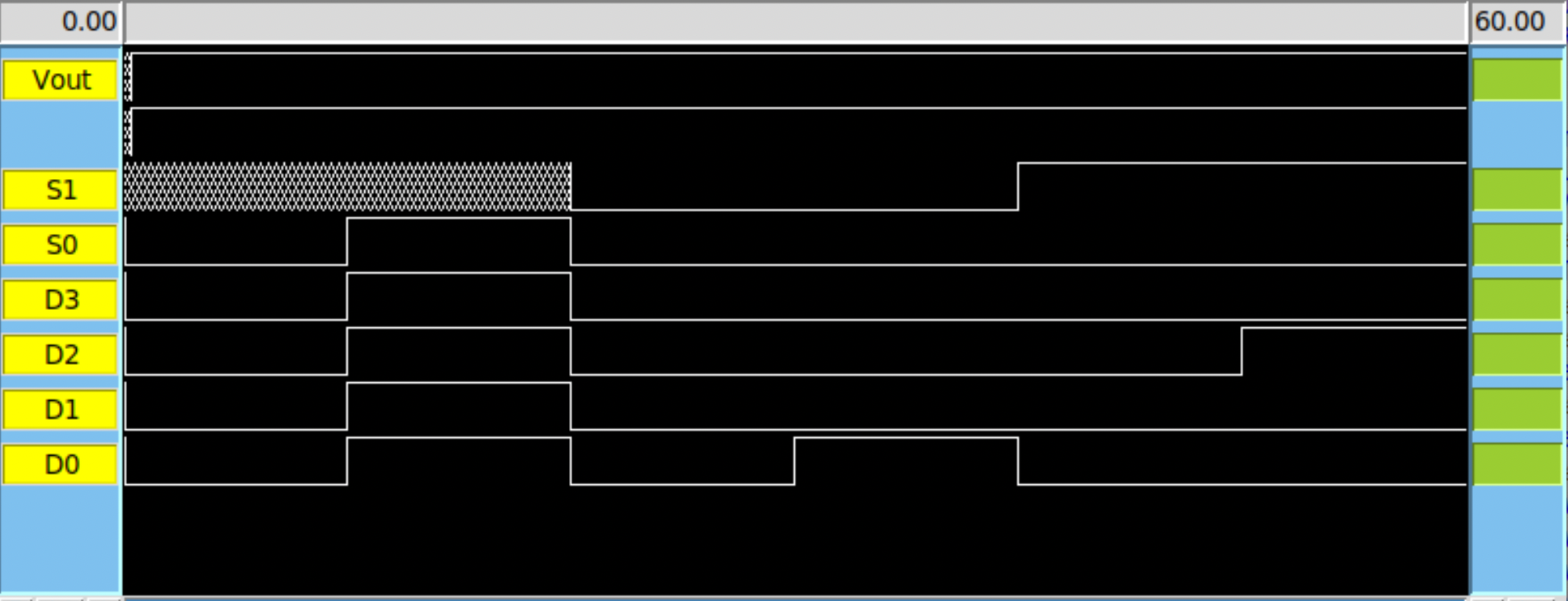
After building the 4:1 Multiplexer I had to utilize IRSIM tools to test if our CMOS generated the 4:1 Multiplexer is running properly. Figure 4 shows the waveform of the 4:1 Multiplexer.

Figure 4: Image of the IRSM waveform and layout

Even though the first and second transistors were working and displaying the Vout correctly, we were unable to adequately display the correct values of Vout. Even though the value of Vout was meant to be 0 when all the values were set to 0, the value we were obtaining was always 1.

We were able to get the waveform of this specific inverter, we still wanted to know the output of the waveform. In table 1 shows the output of the 4:1 Multiplexer or the outcome of it.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| S0 | S1 | D3 | D2 | D1 | D0 | y |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 |

Table 1: Outcome of a 4:1 Multiplexer

**Conclusion:**

We had to create the essential basic cells, which include an inverter and transmission gates. The 4:1 Multiplexer must be implemented using cell hierarchy. To achieve compact physical layouts, our cells should be constructed with the Vdd and GND rails aligned. Each rail should be 8 microns wide, and the Vdd and GND rails in each cell should be 51 microns apart. We created a clear input complementary CMOS static 4:1 multiplexer. A graphic of the 4:1 Multiplexer schematic with transistor sizes should be included in the design. Implement the 4:1 Multiplexer with Magic layout tools and simulate it with IRSIM. We then determine the 4:1 Multiplexer's maximum operational frequency.